GHENT UNIVERSITY

Course Specifications

From the academic year 2020-2021 up to and including the academic year

Digital Electronics (E731036)

Due to Covid 19, the education and assessment methods may vary from the information displayed in the schedules and course details. Any changes will be communicated on Ufora.

Course size *(nominal values; actual values may depend on programme)*

Credits 6.0 **Study time 180 h** **Contact hrs** 60.0h

Course offerings and teaching methods in academic year 2021-2022

A (semester 2)	Dutch	Gent	practicum	24.0h
			lecture	36.0h

Lecturers in academic year 2021-2022

Van Cauwelaert, Dimitri	TW07	staff member
Veelaert, Peter	TW07	lecturer-in-charge

Offered in the following programmes in 2021-2022	**crdts**	**offering**
Bachelor of Science in Engineering Technology(main subject Electronics and ICT Engineering Technology)	6	A
Master of Science in Information Engineering Technology	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology(main subject Electronics Engineering)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology(main subject Embedded Systems)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology(main subject ICT)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology(main subject Electronics Engineering)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology(main subject Embedded Systems)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology(main subject ICT)	6	A

Teaching languages

Dutch

Keywords

Digital systems, VHDL, RTL-design, asynchronous design

Position of the course

The course focuses on the design of complex digital circuits. The students are introduced to high-level description languages (VHDL) and the main methodology for the design of sequential circuits: register-transfer-level design. The emphasis is on generic design and the complexity and scalability of the circuits.

Contents

1. Boolean algebra and logic gates
2. Minimalisation of 2 layer Boolean networks (Quine-McCluskey)
3. Multilayer circuits and technology mapping
4. Synchronous design (Latches, Flipflops, Moore and Mealy machines)
5. Fast adders, multipliers, comparators
6. Generic use of SoP building blocks (Decoders, encoders, multiplexers, switching networks)
7. RTL-design and ASM-charts
8. Asynchronous design (races, cycles, hazards, state reduction, merger graphs)
9. Introduction to VHDL

Initial competences

Being familiar with the components and fundamentals of digital electronics: gates, multiplexers, latches, flipflops, finite state machines, Karnaugh maps. AD and DA conversion.

Final competences

1 To design at RTL level using ASM charts
2 To design digital circuits in VHDL
3 To understand the complexity and scalability of combinatorial and sequential circuits
4 To analyse and design asynchronous circuits

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Practicum, Lecture

Learning materials and price

Syllabus for the theory with handouts of slides. Laboratory assignments on the electronic learning platform, sometimes with solutions. Handouts for introduction to VHDL. Manuals for development boards. Reference sources VHDL.

References

Digital Design, 5th ed., Morris Mano and Michael Ciletti, Prentice-Hall, 2007

Course content-related study coaching

Assessment moments

end-of-term and continuous assessment

Examination methods in case of periodic assessment during the first examination period

Oral examination

Examination methods in case of periodic assessment during the second examination period

Oral examination

Examination methods in case of permanent assessment

Report, Job performance assessment

Possibilities of retake in case of permanent assessment

examination during the second examination period is not possible

Extra information on the examination methods

There is a closed-book exam for the theoretical part. The exam consists of four or five questions. In the second examination it is only possible to resume the oral examination of the theoretical part.

Calculation of the examination mark

- oral examination: 2/3
- lab sessions: 1/3. Participation in all lab sessions is mandatory.