

Processing and Packaging Technologies for Photonic Integration (E030450)

Course size *(nominal values; actual values may depend on programme)*

Credits 4.0

Study time 120 h

Course offerings in academic year 2025-2026

A (semester 2)

English

Gent

Lecturers in academic year 2025-2026

Van Steenberge, Geert

TW06

lecturer-in-charge

Missinne, Jeroen

TW06

co-lecturer

Offered in the following programmes in 2025-2026

[Master of Science in Silicon Photonics](#)

crdts

4

offering

A

Teaching languages

English

Keywords

Semiconductor technologies, packaging

Position of the course

Expose the students to various fabrication and packaging concepts necessary for PICs

Contents

Introduction

iSiPP50G Silicon Photonics Platform

Semiconductor Technologies

Crystal Growth

Silicon Crystal Growth from the Melt

Starting Material

The Czochralski Technique

Distribution of Dopant

Silicon float-zone process

Material Characterization

Wafer Shaping

Crystal Characterization

Silicon Oxidation

Thermal Oxidation Process

Impurity Redistribution During Oxidation

Masking Properties of Silicon Dioxide

Oxide Quality

Oxide Thickness Characterization

Photolithography

Optical Lithography

The Clean Room

Exposure Tools

Masks

Photoresist

Pattern Transfer

Resolution

Next-Generation Lithography Methods

Electron Beam Lithography

Extreme Ultraviolet Lithography

- Etching
 - Wet Chemical Etching
 - Silicon Etching
 - Silicon Dioxide Etching
 - Silicon Nitride Etching
 - Aluminum Etching
 - Dry Etching
 - Plasma Fundamentals
- Etch Mechanism
- Plasma Diagnostics
- End-Point Control
- Reactive Plasma Etching Applications
- Diffusion
 - Basic Diffusion Process
 - Diffusion Equation
- Diffusion Profiles
 - Extrinsic Diffusion
- Ion Implantation
 - Range of Implanted Ions
 - Ion Distribution
- Ion Stopping
- Ion Channeling
 - Implant Damage and Annealing
- Film Deposition
 - Epitaxial Growth Techniques
 - Chemical Vapor Deposition
- Molecular Beam Epitaxy
 - Structures and Defects in Epitaxial Layers
 - Lattice-Matched and Strained-Layer Epitaxy
- Defects in Epitaxial Layers
 - Dielectric Deposition
 - Silicon Dioxide
- Silicon Nitride
 - Metallization
 - Physical Vapor Deposition
- Chemical Vapor Deposition
- Aluminum Metallization
 - Copper Metallization
- Fabrication of Silicon Waveguide Devices
- Silicon-on-Insulator
 - Separation by Implanted Oxygen (SIMOX)
 - Bond and Etch-Back SOI
 - Wafer Splitting
- Selected Components from iSiPP50G Silicon Photonics Platform
 - Silicon Waveguides
- Modulators
- Photodiodes
- Grating couplers
- Packaging Technologies**
- Optical Packaging
 - Fiber-Coupling
 - Grating-Coupling
 - Edge-Coupling
 - Fiber-Array Attach
- V-groove Integration
- Laser Integration
 - Micro-Packaged Lasers
 - Die Bonding
 - Flip-Chip Bonding
 - Transfer Printing
- Micro-Optics Integration
 - 3D Nano-Printing
- High-accuracy Pick-and-Place

Monolithic Micro-Optics Integration
Electrical Packaging
Wire Bonding
Flip-Chip Bumping and Bonding
Hybrid Bonding
Wafer-Level Packaging
 2D Integration Using Organic Interposers
2.5D Integration Using Silicon Interposers with TSVs
3D Integration
Fanout Wafer-Level Packaging
Micro-Chiplets
Thermal Packaging
 Thermal Interface Materials
 Thermo-Electric Cooling

Initial competences

Basic optics and electromagnetics

Final competences

- 1 Understanding of different semiconductor process steps like crystal growth, oxidation, photolithography, etching, diffusion, ion implantation, and film deposition
- 2 Understanding of the fabrication of the most important integrated photonics components
- 3 Understanding of different photonics packaging processes like fiber array attach; laser integration, micro-optics integration, wire and flip-chip bonding, wafer-level packaging, thermal packaging.
- 4 Critical reading and understanding of a scientific article
- 5 Hands-on experience with a number of process steps in a clean room environment.
- 6 Development of a custom PIC package

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Lecture, Practical, Independent work

Extra information on the teaching methods

Lectures, cleanroom project, independent work

Study material

Type: Slides

Name: Slides and course notes used during the course

Indicative price: Free or paid by faculty

Optional: no

Additional information: Available electronically (free)

References

- [1] May, Gary S.; Sze, Simon M. Fundamentals of Semiconductor Fabrication, John Wiley and Sons, 2004.
- [2] C.Y. Chang and S.M. Sze. ULSI Technology, McGraw-Hill, 1996.
- [3] C.Y. Chang and S.M. Sze. ULSI Devices, John Wiley and Sons, 2000.
- [4] S.M. Sze. VLSI Technology, McGraw-Hill, 1988.
- [5] H. Zimmermann. Silicon Optoelectronic Integrated Circuits, Springer, 2004.

Course content-related study coaching

4 researchers

Assessment moments

end-of-term and continuous assessment

Examination methods in case of periodic assessment during the first examination period

Oral assessment

Examination methods in case of periodic assessment during the second examination period

Oral assessment

Examination methods in case of permanent assessment

Oral assessment

Possibilities of retake in case of permanent assessment

examination during the second examination period is possible in modified form

Extra information on the examination methods

- During examination period: oral closed-book assessment.
- During semester: periodic and permanent evaluation. Presentation about a project focusing on fabrication and packaging

Calculation of the examination mark

70% oral exam, 30% presentation.